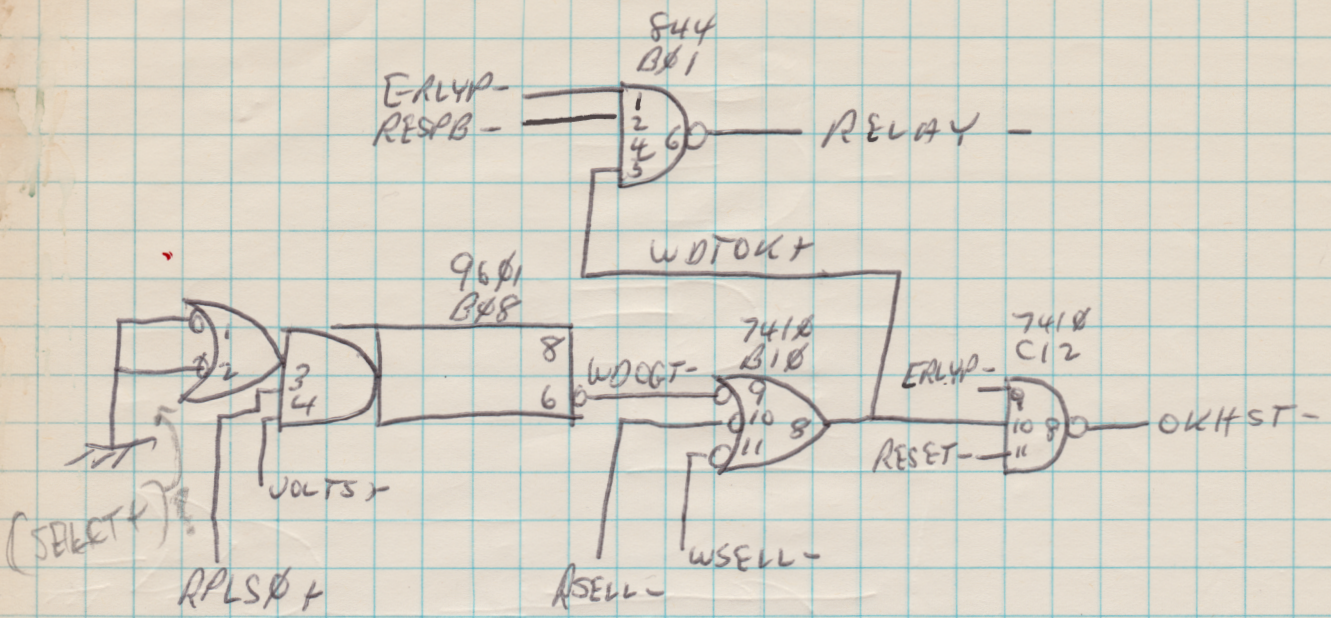
Fix to UCLA Ready Line

NEW



Wiring Changes

delete	BØ8 Ø8	—	C 12 1Ø	2	WDOGT+
delete	BØ1 Ø5	—	BØ8 Ø8	1	WDOGT+
add	B1Ø Ø8	—	BØ1 Ø5	1	WDTOK+
add	B1Ø Ø8	—	C12 1Ø	2	WDTOK+
add	BØ8 Ø6	—	B1Ø Ø9	1	WDOGT-
delete	A18 12	—	A3Ø Ø3	2	SELCT+
delete	A3Ø Ø3	—	BØ8 Ø3	1	SELCT+
add	A18 12	—	A3Ø Ø3	2	SELCT+
add	BØ8 Ø3	—	B 18 Ø5	2	RPLSØ+
delete	A16 Ø9	—	B 19 Ø8	2	RSELL-
add	B19 Ø8	—	B1Ø1Ø	1	RSELL-
add	A16 Ø9	—	B19 Ø8	2	RSELL-
~~add~~	C2013	—	B1Ø 11	2	WSELL-

Wire List Changes - run list

delete	WDOGT+			
add	WDTOK+			
	B1Ø Ø8	—	B Ø1 Ø5	1
	B1Ø Ø8	—	C12 10	2
add	WDOGT-			
	BØ8 Ø6	—	B1Ø Ø9	

delete SELCT+
A30 03 — B08 03 1

add RPLSØ
B08 03 — B18 05 2

add RSELL—
B19 08 — B1Ø 1Ø 1

add WSELL—
C2013 — B1Ø 11 2

Wire List Changes — module list

~~change~~	B01 05	WDTOK+
change	B08 03	APLSØ+
~~deleted~~	B08 06	WDOGT-
delete	B08 08	
add	B1Ø ~~08~~	WDTOK+
add	B1Ø 09	WDOGT-
add	B1Ø 1Ø	RSELL-
add	B1Ø 11	WSELL-
change	C12 1Ø	WDTOK+

Module Layout

B1Ø — 741Ø change to F

Note; Timing for 96Ø1 can be any reasonable interval, Ready line will stay up while an operation is selected and for m seconds after RPLSØ ~~comes~~ ~~true~~ fires where m is the length of WDOGT. Two seconds is perhaps quite reasonable.